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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/617,817	07/14/2003	Toshio Teraishi	03DCOAI030	5232

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EXAMINER	
VELEZ, ROBERTO	
ART UNIT	PAPER NUMBER
2829	
MAIL DATE	DELIVERY MODE
03/17/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/617,817	TERAISHI, TOSHIO	
	Examiner	Art Unit	
	Roberto Velez	2829	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 February 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11 and 16-23* is/are pending in the application.

4a) Of the above claim(s) *4-11 and 16-19* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☒ Claim(s) *20-23* are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *01 June 2007* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *07/14/2003,02/13/2008*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 02/13/2008 has been entered.

Election/Restrictions

2. Newly submitted claims 20-23 are directed to an invention that is independent or distinct from the invention originally claimed for the following reasons: Newly added independent claim 20 recites "a semiconductor device, comprising: a rectangular-shaped voltage output driver LSI chip, which is mounted on the carrier, wherein each of the input leads is electrically connected to one of the input terminals, each-of the output leads is electrically connected to one of the output terminals and the single test signal output lead is electrically connected to the single test signal output terminal, and wherein the input leads and the single test signal output lead are disposed along the first side of the LSI chip, the output leads are disposed along the second side of the LSI chip" which was not disclosed in the original presentation of the original claims. The newly added limitations require search in a different class (714 or 439) and therefore will create a burden on the Examiner. Same argument is applied to dependent claims 21-23, since it depends from independent claim 20.

3. Since applicant has received an action on the merits for the originally presented invention, this invention has been constructively elected by original presentation for prosecution on the merits. Accordingly, claims 20-23 are withdrawn from consideration as being directed to a non-elected invention. See 37 CFR 1.142(b) and MPEP § 821.03.

Response to Arguments

4. Applicant's arguments with respect to claims 1-3 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1 and 3 are rejected under 35 U.S.C. 103(a) as being unpatentable over Van Brunt (US Pat. 4,357,703) in view of Tran et al. (US PGPUB 2002/0109552).

Regarding claim 1, Van Brunt shows (Fig. 1) an LSI chip (Col. 3, Ln 52-54) having a plurality of output terminals, an internal circuit and a test circuit, the test circuit comprising: a single test signal input terminal [21], which receives a test signal (Col. 4, Ln 1-2), for testing the internal circuit; a single test signal output terminal [33]; a shift register [20] having an input terminal, (connection between 40 and 20) which is connected (electrically connected) to the test signal input terminal [21], output bits of the shift register [20] being equal to a number of the output terminals of the LSI chip (shift register 20 has three output bits and there are three LSI chip output terminals 30); and a plurality of switches [23], each of which includes an input terminal (connection between 20 and 23), an output terminal (connection between 23 and 11) and a control terminal (connection between 40 and 23), a number of the switches (23 has three switches) being equal to the number of the output terminals (30 has three output terminals) of the LSI chip, each input terminal of the switches being connected (electrically connected) to one of the output terminals [30] of the LSI chip, the output terminals of the switches [23] being

commonly connected (23 are electrically commonly connected to 33 through 11, 13, 32 and 31) to the test signal output terminal [33], and each control terminal (connection from 40 to 23) of each switch [23] being connected (40 is electrically connected to output bits of the shift register 20 through 23) to one of the output bits of the shift register [20].

Van Brunt fails to disclose a voltage level of one of the output bits of the shift register being different from these of other output bits of the shift register in response to a clock pulse. However, Tran et al. discloses a voltage level of one of the output bits of the shift register being different from these of other output bits of the shift register in response to a clock pulse (Page 1, Paragraph 0015).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the teachings of Tran et al. into the device of Van Brunt by having a voltage level of one of the output bits of the shift register being different from these of other output bits of the shift register in response to a clock pulse. The ordinary artisan would have been motivated to modify Van Brunt in the manner set forth above for the purpose of sequentially or alternatively testing different locations of the internal circuit to precisely locate a faulty location.

Regarding claim 3, Van Brunt shows (Fig. 1) a clock input terminal [41], the clock input signal is inputted to the clock input terminal [41] from an external device (Col. 4, 25-33. Fig. 1 shows that signal inputted into clock input terminal 41 comes from an external device).

7. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Van Brunt (US Pat. 4,357,703) and Tran et al. (US PGPUB 2002/0109552) as applied to claim 1 above, and further in view of Sakaguchi et al. (US Pat. 6,476,789).

Regarding claim 2, Van Brunt discloses everything as claimed above in claim 1.

Van Brunt fails to disclose wherein the LSI chip is an analog voltage output driver LSI chip, and each output terminal of the analog voltage output driver LSI chip outputs an analog

voltage signal. However, Sakaguchi et al. shows (Fig.11) wherein the LSI chip is an analog voltage output driver LSI chip [51], and each output terminal (X01-Z01000) of the analog voltage output driver LSI chip [51] outputs an analog voltage signal (Col. 2, Ln 38-45).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the teachings of Sakaguchi et al. into the device of Van Brunt by having an analog voltage output driver LSI chip, and each output terminal of the analog voltage output driver LSI chip outputs an analog voltage signal. The ordinary artisan would have been motivated to modify Van Brunt in the manner set forth above for the purpose of reducing the cost of the LSI tester by avoiding the usage of a digital voltage output driver LSI chip.

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Sengoku discloses a semiconductor device capable of carrying out high speed fault detecting test.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Roberto Velez whose telephone number is 571-272-8597. The examiner can normally be reached on Monday-Friday 8:00am- 4:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ha Nguyen can be reached on 571-272-1678. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR

system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Roberto Velez/
Examiner, Art Unit 2829

/Ha T. Nguyen/
Supervisory Patent Examiner, Art Unit 2829